[ABSTRACT OF THE DISCLOSURE]

[ABSTRACT]

An electro-luminescence display device and a driving method thereof for assuring a high aperture ratio are disclosed. The electro-luminescence display device includes a plurality of pixel cells arranged in a matrix type, a plurality of data electrodes applying video signals to the pixel cells, and a plurality of gate lines connected to the pixel cells positioned adjacently to each other at the upper/lower sides thereof in such a manner to cross the data electrodes.

[REPRESENTATIVE DRAWING]

FIG. 6

[TITLE OF INVENTION]

ELECTRO-LUMINESCENCE DISPLAY DEVICE AND DRIVING METHOD THEREOF

[BRIEF DESCRIPTION OF DRAWINGS]

[0001] Fig. 1 is a schematic cross-sectional view showing a structure of an organic light-emitting cell in a related electro-luminescence display panel;

[0002] Fig. 2 is a block diagram showing a configuration of a related electro-luminescence display panel;

[0003] Fig. 3 is an equivalent circuit diagram of each pixel cell PE shown in Fig. 2;

[0004] Fig. 4 is a waveform diagram of the gate signals applied to the gate lines shown in Fig. 2;

[0005] Fig. 5 is a block diagram showing a configuration of an electro-luminescence display device according to an embodiment of the present invention;

[0006] Fig. 6 is an equivalent circuit diagram of each pixel cell PE shown in Fig. 5; and

[0007] Fig. 7 is a waveform diagram of the gate signals applied to the gate lines shown in Fig. 5.

[DESCRIPTION OF REFERENCE NUMBER]

2: cathode	4: injection layer
6: electron carrier layer	8: light-emitting layer
10: hole carrier layer	12: hole injection layer
14: anode	16, 40: display panel
18, 19, 44: gate driver	20, 42: data driver
22, 46: pixel cell	50: driving circuit

52: control circuit 100, 102: driving circuit pairs

[DETAILED DESCRITPION OF THE INVENTION]

[OBJECT OF THE INVENTION]

[FIELD OF THE INVENTION AND RELATED ART]

[0008] This invention relates to an electro-luminescence display (ELD), and more particularly to an electro-luminescence display device and a driving method thereof that is adaptive for assuring a high aperture ratio.

[0009] Recently, there have been highlighted various flat panel display devices reduced in weight and bulk that is capable of eliminating disadvantages of a cathode ray tube (CRT). Such flat panel display devices include a liquid crystal display (LCD), a field emission display (FED), a plasma display panel (PDP) and an electro-luminescence (EL) display, etc.

[0010] Fig. 1 is a section view showing a general organic EL structure for explaining a light-emitting principle of the EL display device. Referring to Fig. 1, the organic EL device of the EL display (ELD) is comprised of an electron injection layer 4, an electron carrier layer 6, a light-emitting layer 8, a hole carrier layer 10 and a hole injection layer 12 that are sequentially disposed between a cathode 2 and an anode 14.

[0011] If a voltage is applied between a transparent electrode, that is, the anode 14 and a metal electrode, that is, the cathode 2, then electrons produced from the cathode 2 are moved, via the electron injection layer 4 and the electron carrier layer 6, into the light-emitting layer 8 while holes produced from the anode 14 are moved, via the hole injection layer 12 and the hole carrier layer 10, into the light-emitting layer 10. Thus, the electrons and the holes fed from the electron carrier layer 6 and the hole carrier layer 10, respectively, are collided at the light-emitting layer to be recombined to generate a

light, and this light is emitted, via the transparent electrode (i.e., the anode 14), into the exterior to thereby display a picture.

[0012] Fig. 2 shows a conventional active matrix type EL display device.

[0013] Referring to Fig. 2, the conventional active matrix type EL display device includes an EL display panel 16 having pixel (hereinafter referred briefly to as "PE") cells 22 arranged at each intersection between gate electrode lines GL and data electrode lines DL, first and second gate drivers 18 and 19 for driving the gate electrode lines GL, and a data driver 20 for driving the data electrode lines DL.

[0014] The first gate driver 18 sequentially applies a first gate signal to odd-numbered gate electrode lines GL1, GL3, ... The second gate driver 19 sequentially applies a second gate signal to even-numbered gate electrode lines GL2, GL4, ... Herein, the first and second gate signals are set to have the same width (e.g., 1H), and are applied in such a manner to overlap with each other during a predetermined period.

[0015] The data driver 20 applies video signals corresponding to a data, via the data electrode lines DL, to the PE cells 22. In this case, the data driver 20 applies the video signals for each one horizontal line to the data electrode lines DL every one horizontal period when the first and second gate signals are supplied.

[0016] The PE cells 22 generate a light corresponding to the video signals (i.e., current signals) applied to the data electrode lines DL to thereby display a picture corresponding to the video signals. To this end, as shown in Fig. 3, each PE cell 22 includes a light-emitting cell driving circuit 30 for driving a light-emitting cell OLED in response to a driving signal supplied from each of the data electrode lines DL and the gate electrode lines GL, and a light-emitting cell OLED connected between the light-emitting cell driving circuit 30 and the ground voltage source GND.

[0017] The light-emitting cell driving circuit 30 includes a first driving thin film transistor (TFT) T1 connected between the supply voltage line VDD and the light-emitting cell OELD, a first switching TFT T3 connected between the odd-numbered gate electrode line GLo and the data electrode line DL, a second switching TFT T4 connected between the first switching TFT T3 and the even-numbered gate electrode line GL, a second driving TFT T2 connected between a node positioned between the first and second switching TFT's T3 and T4 and the supply voltage line VDD to form a current mirror circuit with respect to the driving TFT T1, and a storage capacitor Cst connected between a node positioned between the first and second driving TFT's T1 and T2 and the supply voltage line VDD. Herein, the TFT is a p-type electron metal-oxide semiconductor field effect transistor (MOSFET).

[0018] A gate terminal of the first driving TFT T1 is connected to the gate terminal of the second driving TFT T2; a source terminal thereof is connected to the supply voltage line VDD; and a drain terminal thereof is connected to the light-emitting cell OLED. A source terminal of the second driving TFT T2 is connected to the supply voltage line VDD, and a drain terminal thereof is connected to a drain terminal of the first switching TFT T3 and a source terminal of the second switching TFT T4.

[0019] A source terminal of the first switching TFT T3 is connected to the data electrode line DL, and a gate terminal thereof is connected to the odd-numbered gate electrode line GLo. A drain terminal of the second switching TFT T4 is connected to the gate terminals of the first and second driving TFT's T1 and T2 and the storage capacitor Cst. A gate terminal of the second switching TFT T4 is connected to the even-numbered gate electrode line GLe.

[0020] Herein, the first and second driving TFT's T1 and T2 are connected to each other in such a manner to form a current mirror. Thus, assuming that the first and

second driving TFT's T1 and T2 should have the same channel width, a current amount flowing in the first driving TFT T1 is set to be equal to a current flowing in the second driving TFT T2.

[0021] An operation procedure of such a light-emitting cell driving circuit 30 will be described in detail with reference to a driving waveform of Fig. 4 below. First, first and second gate signals SP1 and SP2 having the same width are applied to the odd-numbered electrode line GLo and the even-numbered electrode line GLe making the same horizontal line, respectively, in such a manner to overlap with each other during a predetermined period. Herein, the second gate signal SP2 is applied prior to the first gate signal SP1.

[0022] If the first and second gate signals SP1 and SP2 are supplied, then the first and second switching TFT's T3 and T4 are turned on. As the first and second switching TFT's T3 and T4 are turned on, a video signal from the data electrode line DL is applied, via the first and second switching TFT's T3 and T4, to the gate terminals of the first and second driving TFT's T1 and T2. At this time, the first and second driving TFT's T1 and T2 supplied with the video signals are turned on. Herein, the first driving TFT T1 controls a current flowing from the source terminal thereof (i.e., VDD) into the drain terminal thereof in response to the video signal applied to the gate terminal thereof to apply it to the light-emitting cell OLED, thereby allowing a light having a brightness corresponding to the video signal to be emitted from the light-emitting cell OLED.

[0023] At the same time, the second driving TFT T2 applies a current id fed from the supply voltage line VDD, via the first switching TFT T3, to the data electrode line DL. Herein, since the first and second driving TFT's T1 and T2 form a current mirror circuit, the same current flows in the first and second driving TFT's T1 and T2. Meanwhile, the storage capacitor Cst stores a voltage from the supply voltage line VDD

in such a manner to correspond to an amount of the current id flowing into the second driving TFT T2. Further, the storage capacitor Cst turns on the first driving TFT T1 using a voltage stored therein when the first and second gate signals SP1 and SP2 are inverted into OFF signals (e.g., ground potentials) to turn off the first and second switching TFT's T3 and T4, thereby applying a current corresponding to the video signal to the light-emitting cell OEL. On the other hand, since the second gate signal SP2 is firstly inverted into an OFF signal, that is, the second switching TFT T4 is turned off prior to the first switching TFT T3 in the prior art, it is possible to prevent a voltage charged in the storage capacitor Cst from being discharged into the exterior.

[0024] In real, the conventional EL display device sequentially applies the first and second gate signals SP1 and SP2 to the odd-numbered and even-numbered gate electrode lines GLo and GLe, respectively and applies video signals to the data electrode lines DL, thereby displaying a desired picture. However, such a conventional EL display device has a problem in that, since two gate electrode lines are provided at a single of horizontal line and four TFT's are provided to drive a single of light-emitting cell OELD, an aperture ratio is low. Moreover, the conventional EL display device has a problem in that, since two gate drivers are provided to drive the odd-numbered gate electrode lines GLo and the even-numbered electrode lines GLe, a manufacturing cost rises.

[Technical problems to be resolved by the present invention]

[0025] Accordingly, it is an object of the present invention to provide an electro-luminescence display device and a driving method thereof that is adaptive for assuring a high aperture ratio.

[The construction the present invention]

[0026] In order to achieve these and other objects of the invention, an electro-luminescence display device according to one aspect of the present invention includes a plurality of pixel cells arranged in a matrix type; a plurality of data electrodes for applying video signals to the pixel cells; and a plurality of gate lines connected to the pixel cells positioned adjacently to each other at the upper/lower sides thereof in such a manner to cross the data electrodes.

[0027] The electro-luminescence display device further includes a gate driver for applying a gate signal having a turn-on potential during two horizontal periods to the gate lines.

[0028] Herein, a gate signal applied to the ith gate line (wherein i is an integer) overlaps with a gate signal applied to the (i+1)th gate line during one horizontal period.

[0029] An electro-luminescence display device according to another aspect of the present invention includes electro-luminescence cells arranged in a matrix type at intersections between gate lines and data lines; a supply voltage line for supplying a driving voltage to the electro-luminescence cells; driving circuits for controlling a current applied from the driving voltage of the supply voltage line to the electro-luminescence cells in response to video signals; and control circuits for applying the video signals to the driving circuits.

[0030] In the electro-luminescence display device, each of the driving circuits includes a first driving circuit provided at the ith horizontal line (wherein i is an integer) to apply the current to the electro-luminescence cell positioned at the ith horizontal line, in response to a video signal from the control circuit controlled by the ith gate line, when a gate signal is applied to the (i-1)th gate line; and a second driving circuit provided at the (i+1)th horizontal line to apply the current to the electro-luminescence cell positioned at

the (i+1)th horizontal line, in response to a video signal from the control circuit controlled by the ith gate line, when a gate signal is applied to the (i+1)th gate line.

[0031] Herein, the control circuit is positioned between the first driving circuit and the second driving circuit.

[0032] The second driving circuit provided at the (i-1)th horizontal line is connected to the (i-1)th gate line.

[0033] The first driving circuit provided at the (i+2)th horizontal line is connected to the (i+1)th gate line.

[0034] The first driving circuits includes a first driving thin film transistor having a source terminal connected to the supply voltage line and a drain terminal connected to the electro-luminescence cell positioned at the ith horizontal line; a second driving thin film transistor having a drain terminal connected to a gate terminal of the first driving thin film transistor, a source terminal connected to the control circuit and a gate terminal connected to the (i-1)th gate line; and a first storage capacitor connected between the source terminal and the gate terminal of the first driving thin film transistor.

[0035] The second driving circuits includes a first driving thin film transistor having a source terminal connected to the supply voltage line and a drain terminal connected to the electro-luminescence cell positioned at the (i+1)th horizontal line; a second driving thin film transistor having a drain terminal connected to a gate terminal of the first driving thin film transistor, a source terminal connected to the control circuit and a gate terminal connected to the (i+1)th gate line; and a second storage capacitor connected between the source terminal and the gate terminal of the first driving thin film transistor.

[0036] The control circuit includes a first control thin film transistor having a source terminal connected to the supply voltage line and a drain terminal and a gate terminal connected to the source terminal of the second driving thin film transistor; and a second

control thin film transistor having a drain terminal connected to the gate terminal of the first control thin film transistor, a source terminal connected to the data line and a gate terminal connected to the ith gate line.

[0037] Herein, any one of the first and second control thin film transistors is provided at the ith horizontal line while the remaining one thereof is provided at the (i+1)the horizontal line.

[0038] The electro-luminescence display device further includes a gate driver for applying a gate signal having a turn-on potential during two horizontal periods to the gate lines.

[0039] Herein, a gate signal applied to the ith gate line overlaps with a gate signal applied to the (i+1)th gate line during one horizontal period.

[0040] If a gate signal is applied to the (i-1)th and ith gate lines, then the second driving thin film transistor connected to the (i-1)the gate line and the second control thin film transistor connected to the ith gate line are turned on; and, as the second control thin film transistor is turned on, a video signal from the data line is applied to the first driving thin film transistor and the first control thin film transistor that are positioned at the ith horizontal line.

[0041] Herein, the first driving thin film transistor positioned at the ith horizontal line applies the current corresponding to the video signal to the electro-luminescence cell provided at the ith horizontal line.

[0042] The first control thin film transistor applies the current corresponding to the video signal from the supply voltage line to the data line.

[0043] Herein, a voltage corresponding to the current flowing in the first control thin film transistor is stored in the storage capacitor.

[0044] An electro-luminescence display device according to still another aspect of the present invention includes a plurality of pixel cells arranged in a matrix type; a plurality of data electrodes for applying video signals to the pixel cells; a plurality of gate lines shared with the pixel cells positioned adjacently to each other at the upper/lower sides thereof in such a manner to cross the data electrodes; electro-luminescence cells provided for each pixel cell; a supply voltage line for supplying a driving voltage to the electro-luminescence cells; driving circuits for applying a current corresponding to the video signals to the electro-luminescence cells in response to the video signals; and control circuits connected to the data electrodes to apply the video signals supplied to the data electrodes to the driving circuits.

[0045] The electro-luminescence display device further includes a gate driver for applying a gate signal having a turn-on potential during two horizontal periods to the gate lines.

[0046] Herein, a gate signal applied to the ith gate line (wherein i is an integer) overlaps with a gate signal applied to the (i+1)th gate line during one horizontal period.

[0047] Each of the driving circuits includes a first driving circuit provided at the ith horizontal line (wherein i is an integer) to apply the current to the electro-luminescence cell positioned at the ith horizontal line, in response to a video signal from the control circuit controlled by the ith gate line, when a gate signal is applied to the (i-1)th gate line; and a second driving circuit provided at the (i+1)th horizontal line to apply the current to the electro-luminescence cell positioned at the (i+1)th horizontal line, in response to a video signal from the control circuit controlled by the ith gate line, when a gate signal is applied to the (i+1)th gate line.

[0048] Herein, the control circuit is positioned between the first driving circuit and the second driving circuit.

[0049] A method of driving an electro-luminescence display device according to still another aspect of the present invention includes applying a gate signal having a turn-on potential to gate lines during two horizontal periods, wherein the gate signal applied to the ith gate line (wherein i is an integer) overlaps with the gate signal applied to the (i-1)th gate line during one horizontal period.

[0050] In the method, a current corresponding to a video signal is applied to an electro-luminescence cell provided at the ith horizontal line during the one horizontal period in which the gate signal applied to the (i-1)th gate line overlaps with the gate signal applied to the ith gate line.

[0051] These and other objects of the invention will be apparent from the following detailed description of the embodiments of the present invention with reference to the accompanying drawings

[0052] The description of the embodiments of the present invention is described with reference to Figs. 5 to 7.

[0053] Fig. 5 shows an active matrix type electro-luminescence (EL) display device according to an embodiment of the present invention.

[0054] Referring to Fig. 5, the EL display device includes an EL display panel 40 having pixel (hereinafter referred briefly to as "PE") cells 46 arranged at each intersection between gate electrode lines GL and data electrode lines DL, a gate driver 44 for driving the gate electrode lines GL, and a data driver 42 for driving the data electrode lines DL.

[0055] The gate electrode lines GL are connected to the PE cells 46 positioned at the upper/lower portions thereof. In other words, the ith gate electrode line GLi (wherein i is an integer) is connected to the PE cells 46 provided at the ith horizontal line and the PE cells 46 provided at the (i+1)th horizontal line. Herein, the ith gate electrode line

GLi drives the PE cells 46 provided at the ith and (i+1)th horizontal lines. In other words, the embodiment of the present invention allows a single of gate electrode line GL to drive the PE cells 46 positioned adjacently to each other at the upper/lower portions thereof, it can reduce the number of gate electrode lines GL into a half (1/2) in comparison to the prior art and hence can assure a high aperture ratio. Furthermore, as the embodiment of the present invention has the number of gate electrode lines GL reduced in comparison to the prior art, it can drive the gate electrode lines GL using a single of gate driver 44 and thus can reduce a manufacturing cost.

[0056] As shown in Fig. 7, the gate driver 44 sequentially applies a gate signal having a turn-on potential during two horizontal periods (2H) to the gate electrode lines GL. Herein, a gate signal applied to the ith gate electrode line GLi overlaps with a gate signal applied to the (i-1)th gate electrode line GLi-1 during one horizontal period (1H).

[0057] The data driver 42 applies video signals corresponding to a data, via the data electrode lines DL, to the PE cells 46. Herein, the data driver 42 applies video signals for each one horizontal line to the data electrode lines DL every one horizontal period (1H).

[0058] The PE cells 46 emit a light corresponding to the video signals (i.e., current signals) applied to the data electrode lines DL to thereby display a picture corresponding to the video signals. To this end, the PE cells 46 are configured as shown in Fig. 6.

[0059] Fig. 6 is an equivalent circuit diagram of each pixel cell PE according to an embodiment of the present invention.

[0060] Referring to Fig. 6, the PE cells 46 according to an embodiment of the present invention includes driving circuits 50 for driving the light-emitting cells OLED, and a control circuit 52 for controlling the driving circuits 50 positioned adjacently to each

other at the upper/lower portions thereof. Herein, two driving circuits 50 positioned adjacently to each other at the upper/lower portions thereof makes a pair 100 and 102 (hereinafter referred to "driving circuit pair") to be controlled by a single of control circuit 52. In real, the control circuit 52 controls two driving circuits 50 under control of a single of gate electrode line GL connected thereto.

[0061] The driving circuits 50 is configured for each of the light-emitting cells OELD arranged in a matrix type to thereby make a control such that a current can be applied to each light-emitting cell OLED. The control circuit 52 is provided between the driving circuit pairs 100 and 102 to thereby control the driving circuits 50 positioned adjacently to each other at the upper/lower portions thereof. Herein, the control circuit 52 is provided for each driving circuit pair 100 and 102, so that the number of control circuits 52 included in one vertical line is set to be a half of the number of driving circuits 50.

[0062] On the other hand, the driving circuits 50 positioned adjacently to each other at the upper/lower portions thereof and not provided with the control circuit 52 therebetween are connected to the same gate electrode line. For instance, if the driving circuits 50 provided at the ith and (i+1)th horizontal lines make a driving circuit pair 100 and the driving circuits 50 provided at the (i+2)th and (i+3)th horizontal lines make a driving circuit pair 102, the driving circuits 50 positioned at the (i+1)th horizontal line and the (i+2)th horizontal line are connected to the same gate electrode line.

[0063] The driving circuit 50 provided for each light-emitting cell OLED has two TFT's T1 and T2. For instance, each driving circuit 50 includes a first driving TFT T1 provided between the light-emitting cell OLED and the supply voltage line VDD, and a second driving TFT T2 provided between the first driving TFT T1 and the gate electrode line GL.

[0064] Herein, the gate terminal of the second driving TFT T2 included in the first driving circuit 50 of the driving circuit pair 100, for example, the driving circuit 50 provided at the ith horizontal period is connected to the (i-1)the gate electrode line GLi-1 (wherein, the (i-1)th gate electrode line GLi-1 also is connected to the second driving TFT T2 of the driving circuit 50 provided at the (i-1)th horizontal line), and the source terminal thereof is connected to the control circuit 52 located adjacently. The gate terminal of the first driving TFT T1 included in the driving circuit 50 provided at the ith horizontal line is connected to the drain terminal of the second driving TFT T2, and the source terminal thereof is connected to the supply voltage line VDD. Further, the drain terminal of the first driving TFT T1 is connected to the light-emitting cell OLED1. The storage capacitor Cst is connected between the source terminal and the gate terminal of the first driving TFT T1.

[0065] On the other hand, the gate terminal of the second driving TFT T2 included in the second driving circuit 50 of the driving circuit pair 100, for example, the driving circuit 50 provided at the (i+1)th horizontal period is connected to the (i+1)the gate electrode line GLi+1 (wherein, the (i+1)th gate electrode line GLi+1 also is connected to the second driving TFT T2 of the driving circuit 50 provided at the (i+2)th horizontal line), and the source terminal thereof is connected to the control circuit 52 located adjacently. The gate terminal of the first driving TFT T1 included in the driving circuit 50 provided at the (i+1)th horizontal line is connected to the drain terminal of the second driving TFT T2, and the source terminal thereof is connected to the supply voltage line VDD. Further, the drain terminal of the first driving TFT T1 is connected to the light-emitting cell OLED. The storage capacitor Cst is connected between the source terminal and the gate terminal of the first driving TFT T1. In real, the first and second

driving TFT's T1 and T2 included in the driving circuit pairs 100 and 102 are provided for each light-emitting cell OLED in this manner.

[0066] The control circuit 52 provided between the driving circuit pair 100, for example, the control circuit 52 positioned between the ith and (i+1)th horizontal lines includes a first control TFT T3 and a second control TFT T4. Herein, two TFT's T3 and T4 included in the control circuit 52 are provided in such a manner to be located at different horizontal lines. For instance, the first control TFT T3 is provided to be located at the ith horizontal line while the second control TFT T4 is provided to be located at the (i+1)th horizontal line. Alternatively, the first control TFT T3 may be provided to be located at the (i+1)th horizontal line while the second control TFT T4 may be provided to be located at the ith horizontal line.

[0067] The source terminal of the first control TFT T3 is connected to the supply voltage line VDD, and the drain terminal and the gate terminal thereof are connected to the second driving TFT T2 included in the driving circuits 50 positioned at the upper/lower portions thereof. The source terminal of the second control TFT T4 is connected to the data line DL; the drain terminal thereof is connected to the drain terminal and the gate terminal of the first control TFT T3; and the gate terminal thereof is connected to the ith gate electrode line GLi.

[0068] An operation procedure of the PE cells 46 according to the embodiment of the present invention will be described in detail with reference to a driving waveform of Fig. 7 below.

[0069] First, a gate signal is applied to the (i-1)th gate electrode line GLi-1. A gate signal overlapping with the gate signal supplied to the (i-1)th gate electrode line GLi-1 during one horizontal period (1H) is applied to the ith gate electrode line GLi. As a gate signal is applied to the (i-1)th gate electrode line GLi-1, the second driving TFT T2

positioned at the ith horizontal line is turned on. Further, as a gate signal is applied to the ith gate electrode line GLi, the second control TFT T4 connected to the ith gate electrode line GLi is turned on. As the second control TFT T4 and the second driving TFT T2 are turned on, a video signal from the data electrode line DL is applied to the gate terminals of the first control TFT T3 and the first driving TFT T1. At this time, the first control TFT T3 and the first driving TFT T1 supplied with the video signal are turned on. Herein, the first driving TFT T1 controls a current flowing from the source terminal thereof (i.e., VDD) into the drain terminal thereof in response to the video signal applied to the gate terminal thereof to apply it to the light-emitting cell OLED, thereby allowing a light having a brightness corresponding to the video signal to be emitted from the light-emitting cell OLED1. At the same time, the first control TFT T3 applies a current fed from the supply voltage line VDD, via the second control TFT T3, to the data electrode line DL. Meanwhile, the storage capacitor Cst stores a voltage from the supply voltage line VDD in such a manner to correspond to an amount of the current flowing in the first control TFT T3. Further, the storage capacitor Cst turns on the first driving TFT T1 using a voltage stored therein when the video signal is not applied, thereby applying a current corresponding to the video signal to the light-emitting cell OLED1.

[0070] Thereafter, a gate signal is applied to the (i+1)th gate electrode line GLi+1 in such a manner to overlap with the gate signal applied to the ith gate electrode line GLi. As a gate signal is applied to the (i+1)th gate electrode line GLi+1, the second driving TFT T2 positioned at the (i+1)th horizontal line and the second driving TFT T2 positioned at the (i+2)th horizontal line are turned on. As the second driving TFT T2 positioned at the (i+1)th horizontal line is turned on, a video signal from the data electrode line DL is applied, via the second driving TFT T2 positioned at the (i+1)th

horizontal line, to the gate terminal of the first driving TFT T1, thereby turning on the first driving TFT T1.

[0071] At this time, the first driving TFT T1 positioned at the (i+1)th horizontal line controls a current flowing from the source terminal thereof (i.e., VDD) into the drain terminal thereof in response to the video signal applied to the gate terminal thereof to apply it to the light-emitting cell OLED, thereby allowing a light having a brightness corresponding to the video signal to be emitted from the light-emitting cell OLED1. At the same time, the first control TFT T3 applies a current fed from the supply voltage line VDD that becomes different in accordance with a video signal, via the second control TFT T3, to the data electrode line DL. Meanwhile, the storage capacitor Cst stores a voltage from the supply voltage line VDD in such a manner to correspond to an amount of the current flowing in the first control TFT T3. Further, the storage capacitor Cst turns on the first driving TFT T1 using a voltage stored therein when the video signal is not applied, thereby applying a current corresponding to the video signal to the light-emitting cell OLED2.

[0072] Meanwhile, since a video signal fails to be applied to the light-emitting cell OLED3 positioned at the (i+2)th horizontal line even though a gate signal applied to the (i+1)the gate electrode line Gli+1 turns on the second driving TFT T2 positioned at the (i+2)th horizontal line, the second control TFT T4 positioned between the driving circuit pair 102 is turned off and thus a light is not emitted from the light-emitting cell OLED3 positioned at the (i+2)th horizontal line.

[0073] Hereinafter, a gate signal is applied to the (i+2)th gate electrode line GLi+2 in such a manner to overlap with the gate signal applied to the (i+1)th gate electrode line Gli+1. As a gate signal is applied to the (i+2)th gate electrode line Gli+2, the second control TFT T4 connected to the (i+2)th gate electrode line Gli+2 is turned on. As the

second control TFT T4 is turned on, a video signal from the data electrode line DL turns on the first control TFT T3 connected to the second control TFT T4 and the first driving TFT T1 positioned at the (i+2)th horizontal line.

[0074] At this time, the first driving TFT T1 positioned at the (i+2)th horizontal line controls a current flowing from the source terminal thereof (i.e., VDD) into the drain terminal thereof in response to the video signal applied to the gate terminal thereof to apply it to the light-emitting cell OLED3, thereby allowing a light having a brightness corresponding to the video signal to be emitted from the light-emitting cell OLED3. At the same time, the first control TFT T3 applies a current fed from the supply voltage line VDD, via the second control TFT T4, to the data electrode line DL. Meanwhile, the storage capacitor Cst stores a voltage from the supply voltage line VDD in such a manner to correspond to an amount of the current flowing in the first control TFT T3. Further, the storage capacitor Cst turns on the first driving TFT T1 using a voltage stored therein when the video signal is not applied, thereby applying a current corresponding to the video signal to the light-emitting cell OLED3. In real, the present EL display device repeats the above-mentioned procedure to thereby display a desired picture.

[0075] Such an EL display device provides a single of control circuit between the driving circuit pair positioned adjacently to each other at the upper/lower portions thereof and controls the driving circuit positioned at the upper/lower sides while controlling the control circuit by a single of gate electrode line, so that it can reduce the number of gate electrode lines. In other words, since the driving circuit provided at the upper side of the driving circuit pair is connected to the same gate electrode line as the driving circuit provided at the previous horizontal line while the driving circuit provided at the lower side of the driving circuit pair is connected to the same gate

electrode line as the driving circuit provided at the next horizontal line, it becomes possible to minimize the number of gate electrode line and thus to improve an aperture ratio. Furthermore, three TFT's (i.e., two at the driving circuit plus one at the control circuit) are provided for each light-emitting cell arranged in a matrix type, it becomes possible to more improve an aperture ratio.

[The effect of the invention]

[0076] As described above, according to the present invention, the gate electrode lines control the pixel cells positioned at the upper/lower sides, so that it becomes possible to reduce the number of gate lines and thus to improve an aperture ratio. Furthermore, according to the present invention, three TFT's are included for each pixel cell, so that it becomes possible to more improve an aperture ratio in comparison to the prior art. Moreover, according to the present invention, the number of gate electrode lines are reduced, so that it becomes possible to apply a gate signal to all the gate electrode lines using a single of gate driver and thus to reduce a manufacturing cost.

[0077] Although the present invention has been explained by the embodiments shown in the drawings described above, it should be understood to the ordinary skilled person in the art that the invention is not limited to the embodiments, but rather that various changes or modifications thereof are possible without departing from the spirit of the invention. Accordingly, the scope of the invention shall be determined only by the appended claims and their equivalents.

What is claimed is:

1. An electro-luminescence display device, comprising:

a plurality of pixel cells arranged in a matrix type;

a plurality of data electrodes for applying video signals to the pixel cells; and

a plurality of gate lines connected to the pixel cells positioned adjacently to each other at the upper/lower sides thereof in such a manner to cross the data electrodes.

2. The electro-luminescence display device according to claim 1, further comprising:

a gate driver for applying a gate signal having a turn-on potential during two horizontal periods to the gate lines.

3. The electro-luminescence display device according to claim 2, wherein a gate signal applied to the ith gate line (wherein i is an integer) overlaps with a gate signal applied to the (i+1)th gate line during one horizontal period.

4. An electro-luminescence display device, comprising:

electro-luminescence cells arranged in a matrix type at intersections between gate lines and data lines;

a supply voltage line for supplying a driving voltage to the electro-luminescence cells;

driving circuits for controlling a current applied from the driving voltage of the supply voltage line to the electro-luminescence cells in response to video signals; and

control circuits for applying the video signals to the driving circuits.

5. The electro-luminescence display device according to claim 4, wherein each of the driving circuits includes:

a first driving circuit provided at the ith horizontal line (wherein i is an integer) to apply the current to the electro-luminescence cell positioned at the ith horizontal line, in response to a video signal from the control circuit controlled by the ith gate line, when a gate signal is applied to the (i-1)th gate line; and

a second driving circuit provided at the (i+1)th horizontal line to apply the current to the electro-luminescence cell positioned at the (i+1)th horizontal line, in response to a video signal from the control circuit controlled by the ith gate line, when a gate signal is applied to the (i+1)th gate line.

6. The electro-luminescence display device according to claim 5, wherein the control circuit is positioned between the first driving circuit and the second driving circuit.

7. The electro-luminescence display device according to claim 5, wherein the second driving circuit provided at the (i-1)th horizontal line is connected to the (i-1)th gate line.

8. The electro-luminescence display device according to claim 5, wherein the first driving circuit provided at the (i+2)th horizontal line is connected to the (i+1)th gate line.

9. The electro-luminescence display device according to claim 5, wherein the first driving circuits includes:

a first driving thin film transistor having a source terminal connected to the supply voltage line and a drain terminal connected to the electro-luminescence cell positioned at the ith horizontal line;

a second driving thin film transistor having a drain terminal connected to a gate terminal of the first driving thin film transistor, a source terminal connected to the control circuit and a gate terminal connected to the (i-1)th gate line; and

a first storage capacitor connected between the source terminal and the gate terminal of the first driving thin film transistor.

10. The electro-luminescence display device according to claim 5, wherein the second driving circuits includes:

a first driving thin film transistor having a source terminal connected to the supply voltage line and a drain terminal connected to the electro-luminescence cell positioned at the (i+1)th horizontal line;

a second driving thin film transistor having a drain terminal connected to a gate terminal of the first driving thin film transistor, a source terminal connected to the control circuit and a gate terminal connected to the (i+1)th gate line; and

a second storage capacitor connected between the source terminal and the gate terminal of the first driving thin film transistor.

11. The electro-luminescence display device according to claim 9 or 10, wherein the control circuit includes:

a first control thin film transistor having a source terminal connected to the

supply voltage line and a drain terminal and a gate terminal connected to the source terminal of the second driving thin film transistor; and

a second control thin film transistor having a drain terminal connected to the gate terminal of the first control thin film transistor, a source terminal connected to the data line and a gate terminal connected to the ith gate line.

12. The electro-luminescence display device according to claim 11, wherein any one of the first and second control thin film transistors is provided at the ith horizontal line while the remaining one thereof is provided at the (i+1)the horizontal line.

13. The electro-luminescence display device according to claim 11, further comprising:

a gate driver for applying a gate signal having a turn-on potential during two horizontal periods to the gate lines.

14. The electro-luminescence display device according to claim 13, wherein a gate signal applied to the ith gate line overlaps with a gate signal applied to the (i+1)th gate line during one horizontal period.

15. The electro-luminescence display device according to claim 13, wherein, if a gate signal is applied to the (i-1)th and ith gate lines, then the second driving thin film transistor connected to the (i-1)the gate line and the second control thin film transistor connected to the ith gate line are turned on; and

if the second control thin film transistor is turned on, a video signal from the

data line is applied to the first driving thin film transistor and the first control thin film transistor that are positioned at the ith horizontal line.

16. The electro-luminescence display device according to claim 15, wherein the first driving thin film transistor positioned at the ith horizontal line applies the current corresponding to the video signal to the electro-luminescence cell provided at the ith horizontal line.

17. The electro-luminescence display device according to claim 15, wherein the first control thin film transistor applies the current corresponding to the video signal from the supply voltage line to the data line.

18. The electro-luminescence display device according to claim 17, wherein a voltage corresponding to the current flowing in the first control thin film transistor is stored in the storage capacitor.

19. An electro-luminescence display device, comprising:

a plurality of pixel cells arranged in a matrix type;

a plurality of data electrodes for applying video signals to the pixel cells;

a plurality of gate lines shared with the pixel cells positioned adjacently to each other at the upper/lower sides thereof in such a manner to cross the data electrodes;

electro-luminescence cells provided for each pixel cell;

a supply voltage line for supplying a driving voltage to the electro-luminescence cells;

driving circuits for applying a current corresponding to the video signals to the

electro-luminescence cells in response to the video signals; and

control circuits connected to the data electrodes to apply the video signals supplied to the data electrodes to the driving circuits.

20. The electro-luminescence display device according to claim 19, further comprising:

a gate driver for applying a gate signal having a turn-on potential during two horizontal periods to the gate lines.

21. The electro-luminescence display device according to claim 20, wherein a gate signal applied to the ith gate line (wherein i is an integer) overlaps with a gate signal applied to the (i+1)th gate line during one horizontal period.

22. The electro-luminescence display device according to claim 21, wherein each of the driving circuits includes:

a first driving circuit provided at the ith horizontal line (wherein i is an integer) to apply the current to the electro-luminescence cell positioned at the ith horizontal line, in response to a video signal from the control circuit controlled by the ith gate line, when a gate signal is applied to the (i-1)th gate line; and

a second driving circuit provided at the (i+1)th horizontal line to apply the current to the electro-luminescence cell positioned at the (i+1)th horizontal line, in response to a video signal from the control circuit controlled by the ith gate line, when a gate signal is applied to the (i+1)th gate line.

23. The electro-luminescence display device according to claim 22, wherein the

control circuit is positioned between the first driving circuit and the second driving circuit.

24. The electro-luminescence display device according to claim 22, wherein the second driving circuit provided at the (i-1)th horizontal line is connected to the (i-1)th gate line.

25. The electro-luminescence display device according to claim 22, wherein the first driving circuit provided at the (i+2)th horizontal line is connected to the (i+1)th gate line.

26. A method of driving an electro-luminescence display device, comprising the step of:

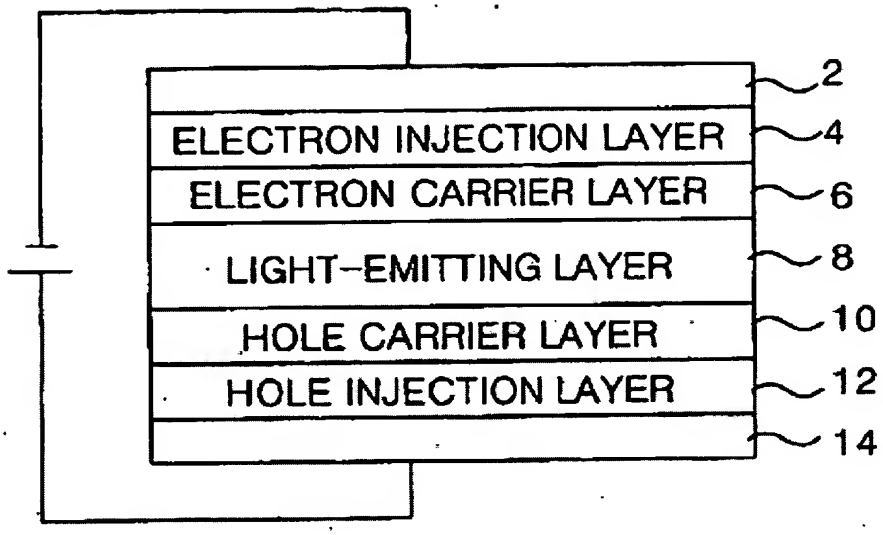
applying a gate signal having a turn-on potential to gate lines during two horizontal periods,

wherein the gate signal applied to the ith gate line (wherein i is an integer) overlaps with the gate signal applied to the (i-1)th gate line during one horizontal period.

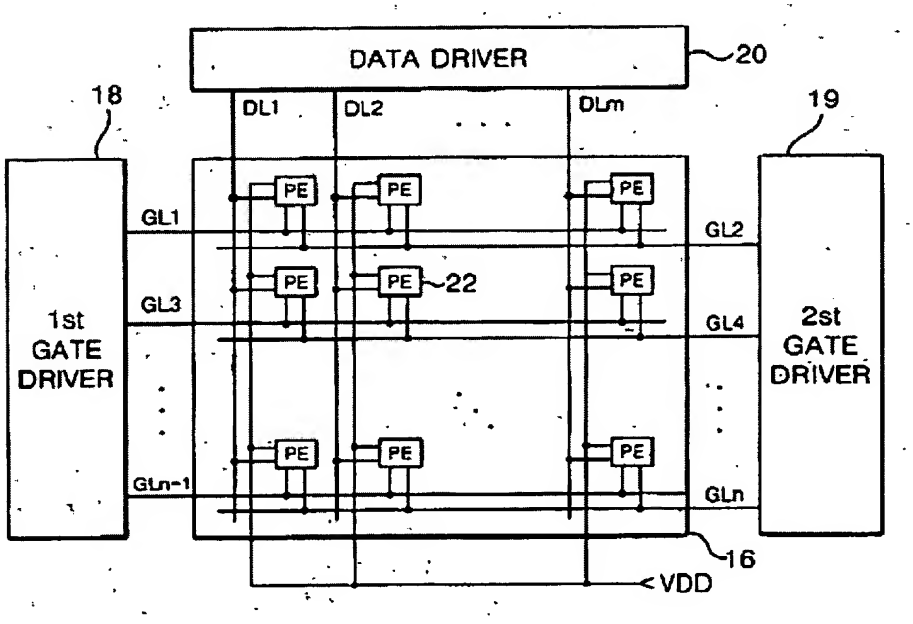
27. The method according to claim 24, wherein a current corresponding to a video signal is applied to an electro-luminescence cell provided at the ith horizontal line during the one horizontal period in which the gate signal applied to the (i-1)th gate line overlaps with the gate signal applied to the ith gate line.

[DRAWINGS]

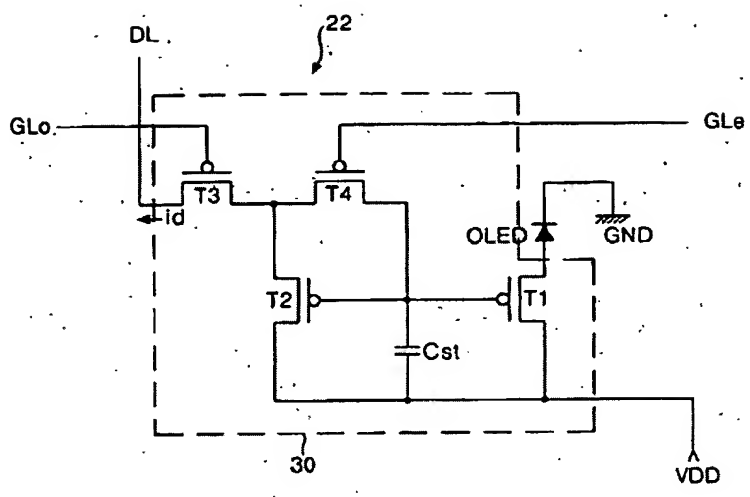
[FIG. 1]



[FIG. 2]



[FIG. 3]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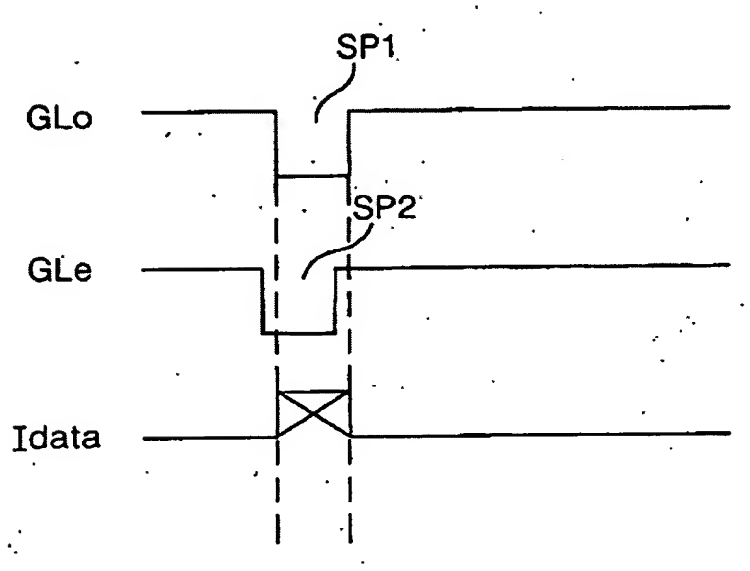
[FIG. 4]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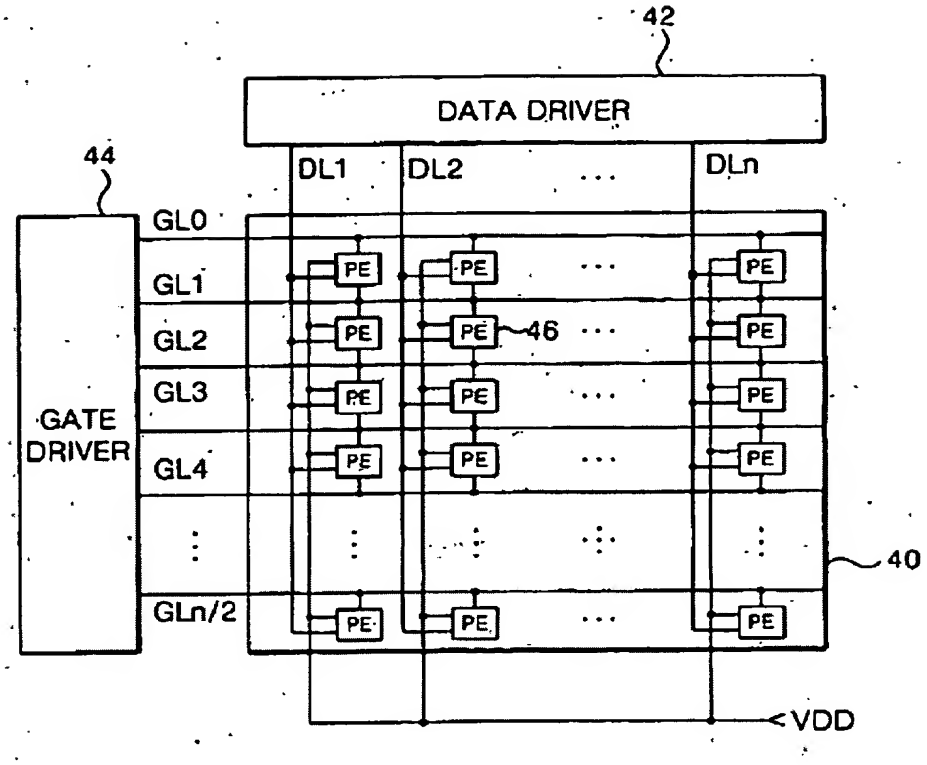
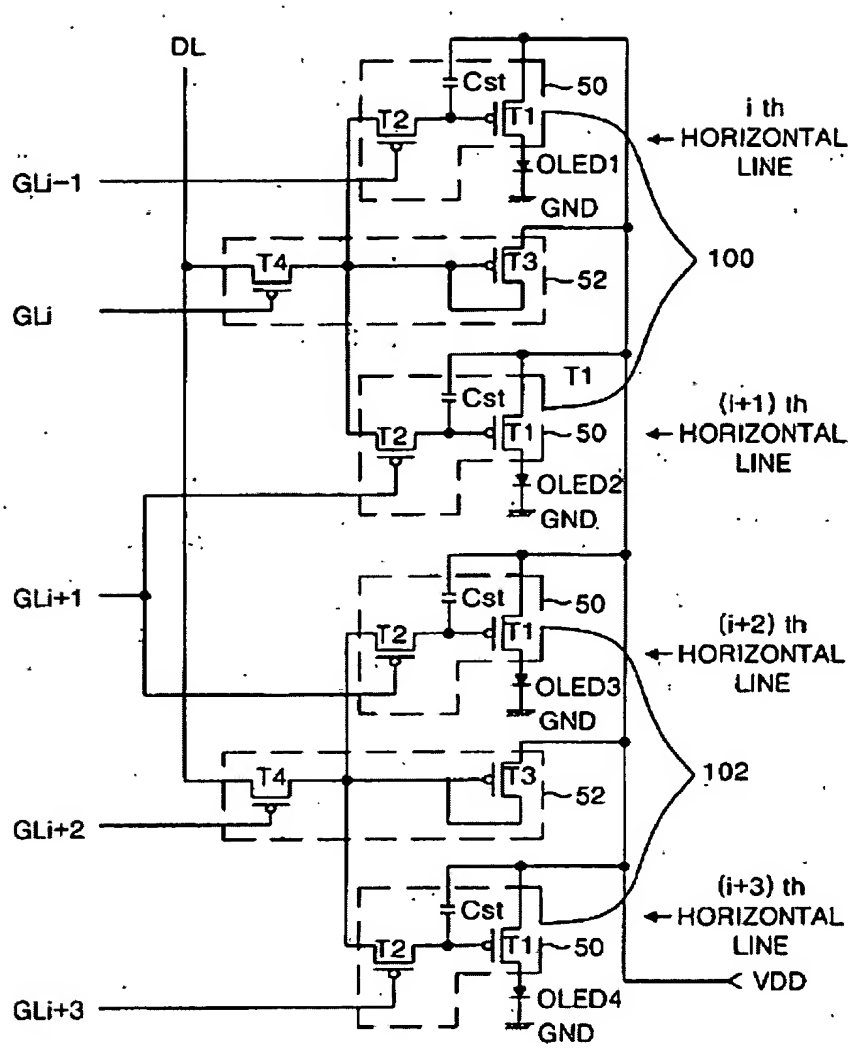
SP2
GLe
Idata

[FIG. 5]


42
DATA DRIVER
44
DL1
DL2
DLn
GL0
GL1
GL2
GL3
GL4
GLn/2
GATE DRIVER
PE
46
40
VDD

[FIG. 6]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T1
Cst
(i+1) th
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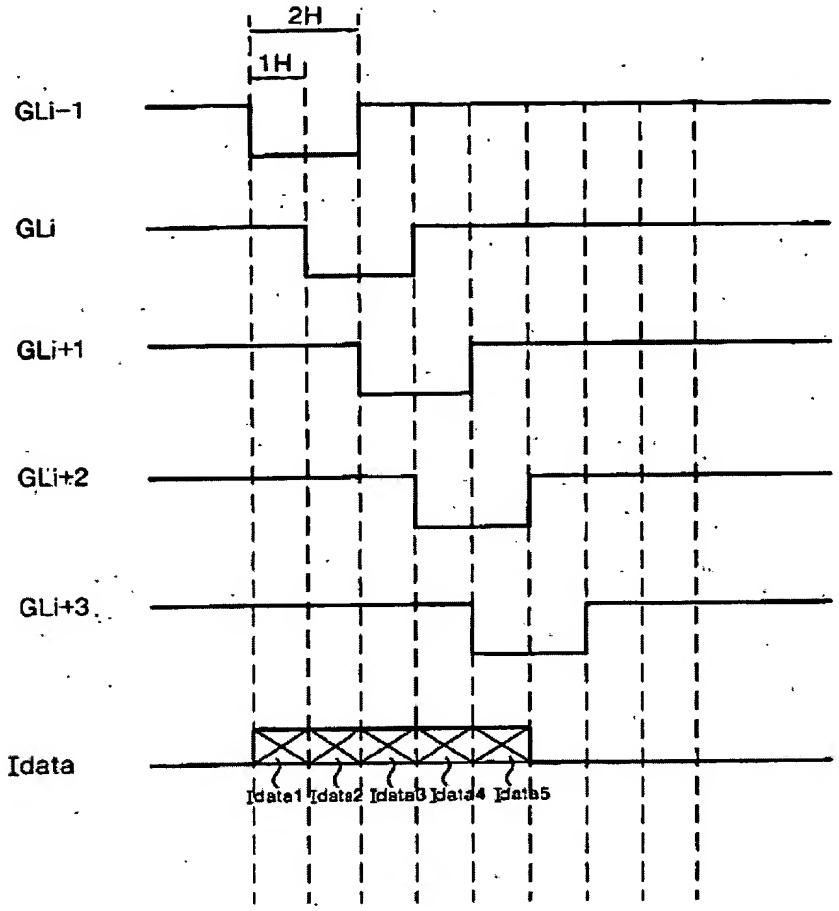
[FIG. 7]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GLi
GLi+1
GLi+2
GLi+3
Idata
Idata1
Idata2
Idata3
Idata4
Idata5

DECLARATION

I, Seung Kyu LEE, hereby declare the following:

I am knowledgeable in Korean and English. I have reviewed Korean Patent Application No.10-2003-0083944 and believe the attached documents to be an accurate translations thereof.

All statements made herein of my own knowledge are true and all statements made on information and belief are believed to be true. Further, these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Seungkyu Lee

Date & Signature: Seung Kyu LEE